

RECORD OF TELEPHONIC INTERVIEW

On May 13, 2004, an interview was conducted with Primary Examiner Kenneth Wells. Andoh, et al. (U.S. 5.936,466) was discussed with respect to the rejection of the Claims in the above-referenced Office Action. No agreement was reached with respect to the Claims. However, the Primary Examiner agreed that the reference signal of Andoh is not a data signal. The Primary Examiner further indicated that the Claims of this application may be subject to an obviousness-type double-patenting rejection in view of the parent application.

REMARKS

Claims 1-18 are currently pending in the application.

1. Corrections to the Specification

The Primary Examiner has objected to the specification in the parent case, indicating informalities. The specification in the instant case has been Amended to correct the informalities as indicated by the Primary Examiner in the parent.

2. Objections to the Drawings

The Primary Examiner has objected to Figure 2 as having a reference designator inconsistency. A replacement sheet for Figure 2 is attached having corrected reference designators.

3. Objections to the Claims

The Primary Examiner has objected to claims 1 and 10, indicating informalities. Claims 1 and 10 have has been Amended to correct the informalities as indicated by the Primary Examiner. Therefore it is believed that the Primary Examiner's objections to the Claims have been overcome.

4. Rejections under 35 U.S.C. §102(b)

The Primary Examiner has rejected Claims 1-6, 8-14 16 and 17 under 35 U.S.C. §102(b) as being anticipated by Andoh. Applicants respectfully disagree, but have Amended the Claims to more particularly point out features of the present invention. Amended Claim 1 recites a "single-ended comparator for comparing an analog value of said single-ended data signal with said reference value, and having an output representative of a digital binary state of said single-ended data signal, whereby said single-ended signal is detected in conformity with a common mode value of said differential signal pair."

Andoh does not disclose such a comparator for detecting a value corresponding to a binary state of a single-ended data signal in conformity with a differential pair common-mode value. Andoh discloses an op-amp (transconductance amp) that includes a feedback circuit having a reference voltage input. The Primary Examiner indicated in the above-referenced Office Action, that the gate of FET 11 of Andoh is read on by the single-ended input recited in Claim 1. Applicants respectfully point out that the indicated gate (input) is for connection of a DC reference voltage that is used to correct the output of the prior art op-amp disclosed in Andoh for the common-mode variation of the signal inputs of the op-amp. The feedback circuit 13 shown in Andoh does not detect a binary value of a single-ended data signal in conformity with a common mode value of a differential signal pair. Feedback circuit 13 does not receive a data signal input at all, and therefore does not compare a single-ended data signal to a reference value, nor detect a binary logic state of a data signal in conformity with a common-mode voltage of a differential data signal pair. Therefore, Andoh does not disclose the interface of Claim 1, nor of dependent claims 2-9.

Similarly, Claim 10 recites "comparing an analog value of said single-ended signal to said reference value, whereby a binary logic state of said single-ended signal is detected in conformity with analog values of both signals of said differential signal pair." As

pointed out above, Andoh does not disclose a circuit or for performing such comparison or detection, and therefore does not disclose the method recited in Claim 10, nor dependent Claim 11-15. Applicants believe that the rejection under 35 U.S.C. §102(b) has been overcome.

Therefore, for all of the reasons stated above, applicants believe that all of the rejections and objections have been overcome.

CONCLUSION

In conclusion, Applicants respectfully submit that this Amendment, in view of the Remarks offered in conjunction therewith, are fully responsive to all aspects of the objections and rejections tendered by the Examiner in the Office Action. Applicants respectfully submit that they have persuasively demonstrated that the above-identified Patent Application, including Claims 1-18 are in condition for allowance. Such action is earnestly solicited.

No fees should be incurred by this Amendment, but if there are any fees incurred by this Amendment Letter, please deduct them from IBM Deposit Account NO. 09-0447.

Respectfully submitted,



Andrew M. Harris
Reg. No. 42,638
(706)-782-9683

Weiss, Moy & Harris, P.C.
4204 North Brown Ave.
Scottsdale, AZ 85251